HEWLETT PACKARD

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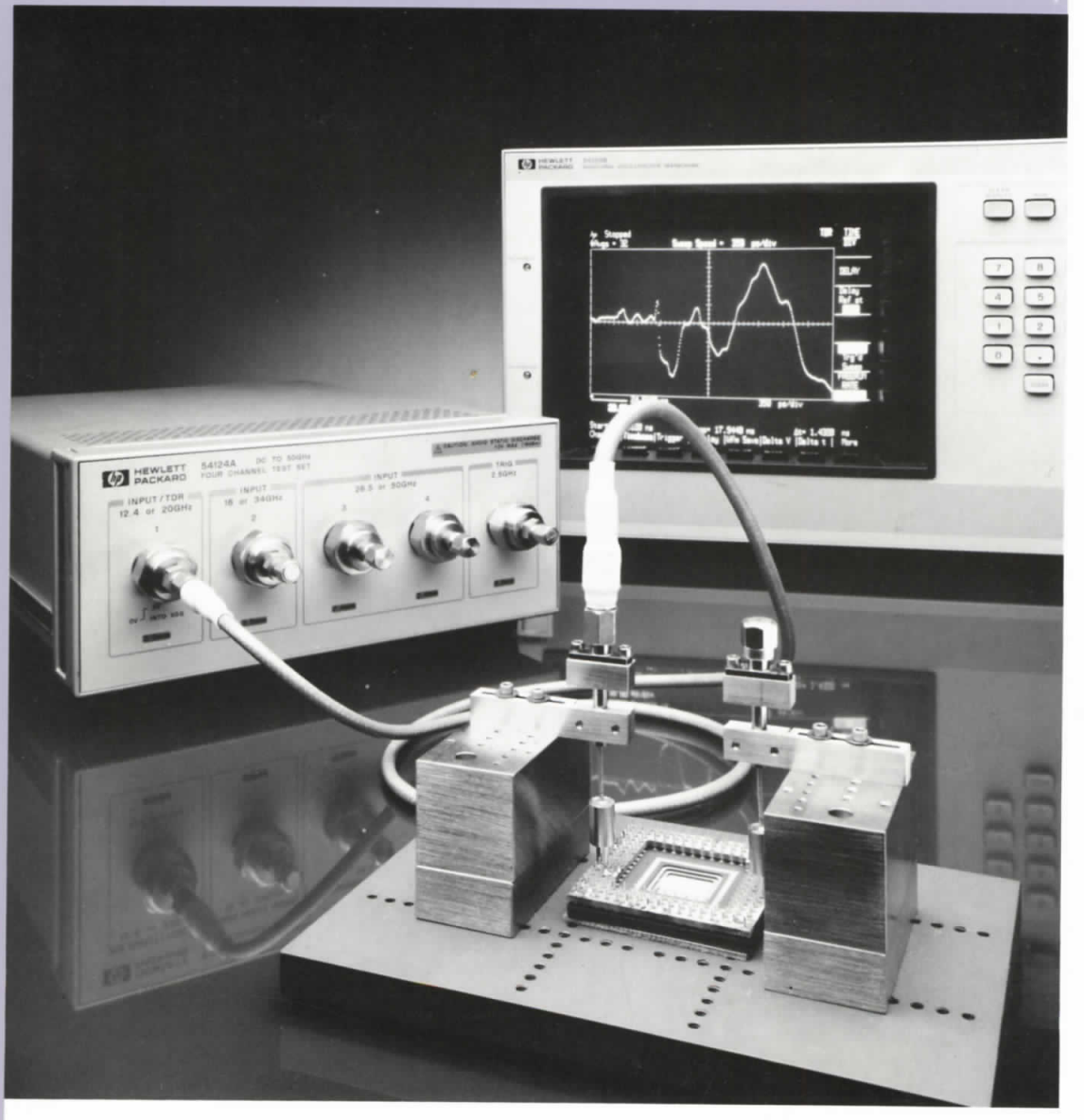


# Advanced TDR Techniques

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## Abstract

RF, microwave, and high speed digital designers can benefit from the use of Time Domain Reflectometry (TDR) to analyze signal integrity through transmission paths. In this application note, you will learn about TDR in various environments including PC boards/backplanes, wafers/hybrids, IC packages, connectors, and cables. Finally, you will also read about evaluating balanced lines using differential TDR. You will learn how to attach to a wide range of possible DUT environments, what TDR performance to expect, and how to optimize the performance.

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## Introduction

Interest in Time Domain Reflectometry (TDR) as a tool for analyzing transmission paths has continued to increase in recent years, both for analog and digital applications. Many questions arise regarding practical issues for TDR measurements like launching techniques and required TDR resolution for various environments. Such questions will be considered in this paper for the use with the HP 54120-series digitizing oscilloscopes in advanced TDR applications.

Some of the most common questions include "how do I hook up my TDR to the non-coaxial DUT?", "what size reflections are typical for a termination resistor?", "how do I probe for transmission signals?", and "are there optimal calibration techniques?" The list goes on and on.

Let's address these topics in the following way. First, a quick review of the basics will provide for a common base of knowledge. Next, the subject of connecting a TDR to a DUT (launching) will be considered. Many types of DUT environments must be considered like PC boards, IC packages, and cables. In each case, launching options, required TDR performance, and typical results will be considered. Finally, two special subjects, calibration and non-50 Ω device-under-tests (DUT's) will receive special attention.

## Section I - TDR Fundamentals

Fundamentals are included in this handout as reference material and should prove helpful for a review when considering advanced topics which follow. See Hewlett-Packard Application Notes 62 and 62-1 for more thorough analysis of TDR basics.

In its most basic description, TDR involves introducing a fast edge step to a transmission system, and then observing the size and location of reflected energy from that incident step. We see responses from a short, 50 Ω load, and open circuit in figure 1. TDR then becomes a tool to view of impedance as a function of distance.

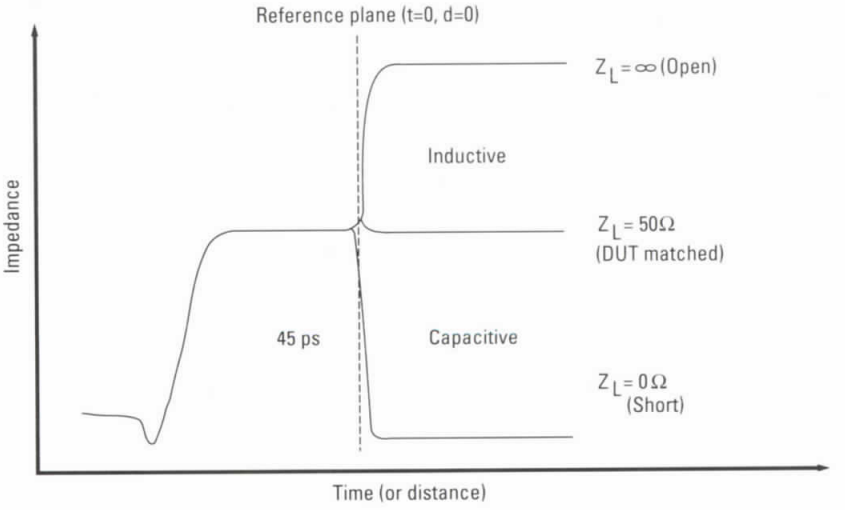



**Figure 1. Time domain reflectometry (TDR)**

A very simple equation relates the size and polarity of a reflected step as a function of a simple resistive load, described in figure 2.

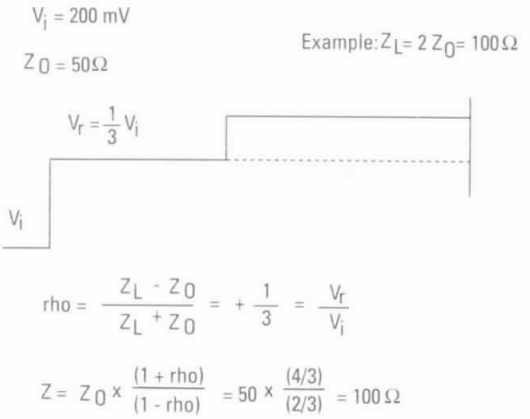



**Figure 2. Resistive TDR equations**

Equations for ideal TDR responses to complex loads can be derived, allowing one to determine R, L, and C values in a circuit. Response time constant and final value are usually the most important factors for such calculations. Some typical responses can be seen in figure 3. For example, with a series RL circuit, with a measured time constant $\tau$ of 20 ps, and a final value of 150 mV from a 200 mV input : R = 30 Ω, and L = 1.6 nH.

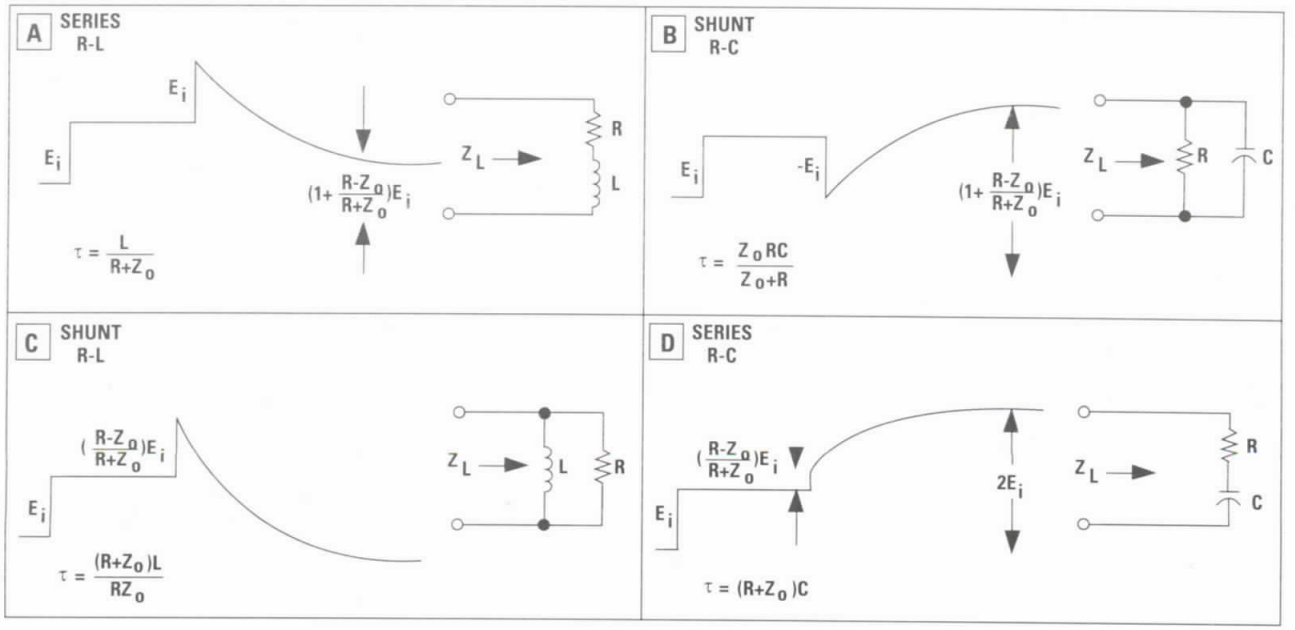



**Figure 3. TDR responses to complex loads**

In a practical TDR measurement, the TDR risetime is finite and the measurement is thus limited in bandwidth. Typical circuit discontinuities along a transmission line have time constants much faster

than the TDR risetime. Thus changing the ideal response to an impulse response, as shown in figure 4 with a series RL circuit.

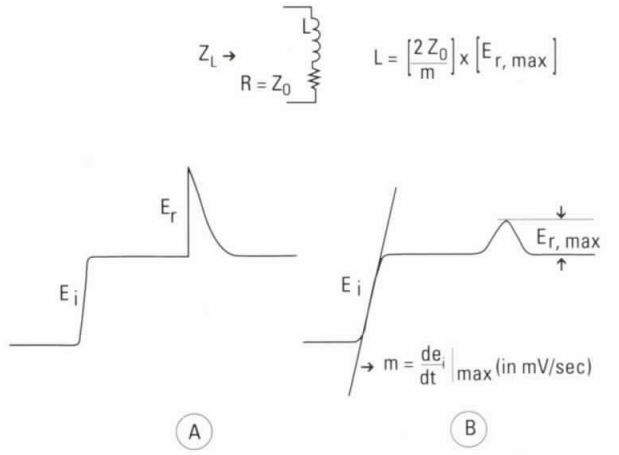



**Figure 4. Ideal "A" versus actual "B" displays of reflection from a small inductor in series with $R = Z_O$**

When the circuit time constant is much less than the TDR risetime the following equation applies:

$$L = \left(\frac{2 Z_O}{m}\right) \times \left(e_{R,\ max}\right)$$

A similar derivation will show a shunt RC circuit, as shown in figure 5. If the circuit and the TDR time constants are similar, response will not respond as impulses and one must approximate circuit values using SPICE analysis.

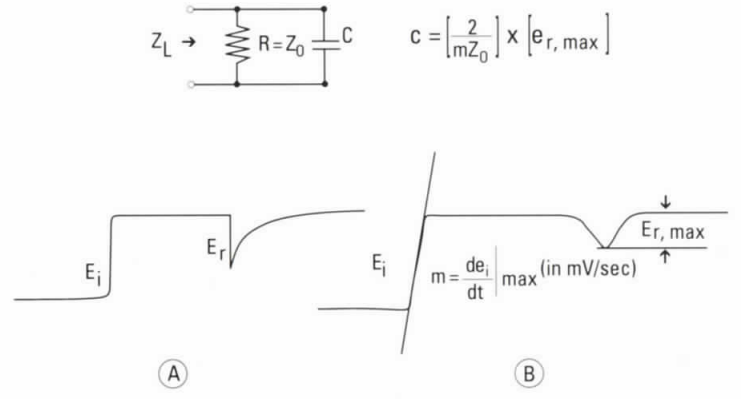



**Figure 5. Ideal "A" versus actual "B" displays of reflection from a small capacitor in shunt with $R = Z_O$**

The TDR is realized in hardware by creating the input step in channel 1 of a HP 54120-series sampling oscilloscope and observing reflections on that same channel like as shown in figure 6. The TDR is calibrated with a standard short and 50 Ω load. This references voltages to impedances and establishes a time reference plane.

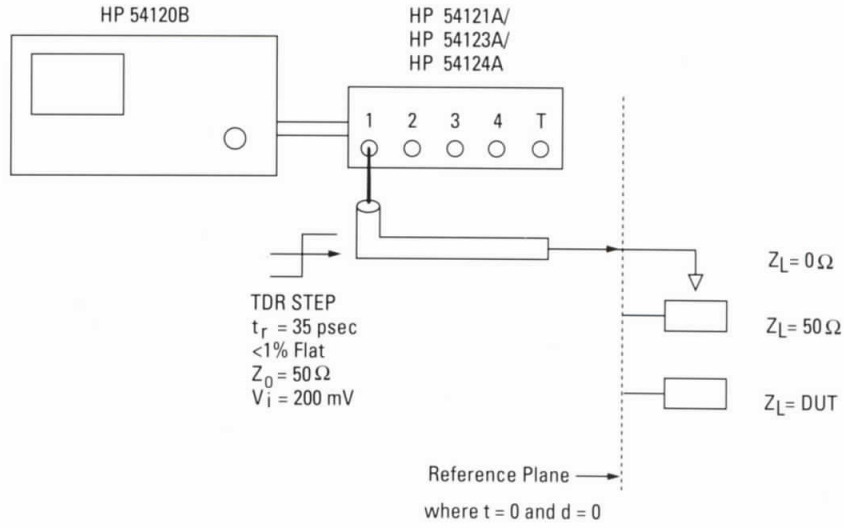



**Figure 6. Time domain reflectometry**

The real power of the TDR then comes in being able to spatially resolve different parts of a DUT in terms of impedance and reflections, with a cursor referenced to the short and 50 Ω standards. Figure 7 demonstrates inductive and capacitive discontinuities along a line and how they effect the TDR response.

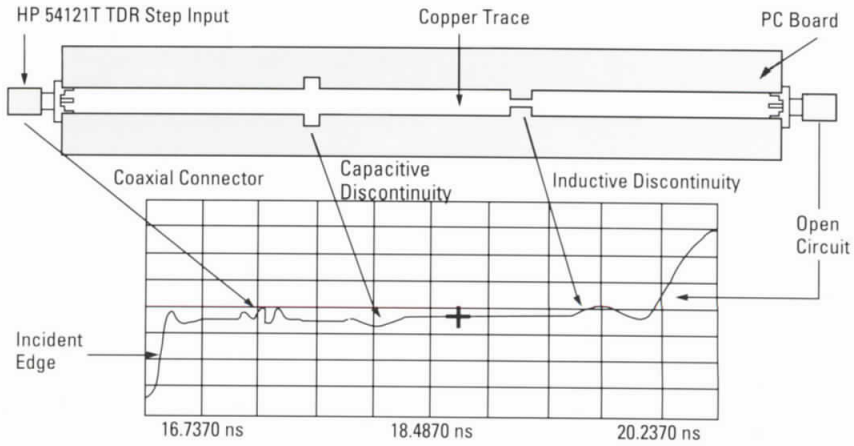
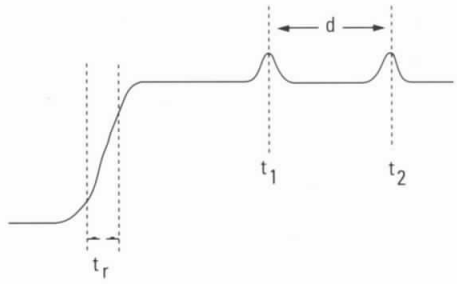



**Figure 7. Typical performance characteristics**

The TDR cursor (indicated in Figure 7 by a "+") provides direct readout of Ω, % reflection, time, and distance from the reference plane.

One of the most important characteristics of a TDR is its ability to distinguish two reflections in distance like in figure 8. This is a direct function of the TDR "system" risetime. If two small discontinuities of equal size are separated by a distance which corresponds to equal to or less than one half the TDR system risetime, the responses merge together. A conservative definition for TDR spatial resolution is therefore "one" system risetime. The system risetime of a TDR is most easily seen by looking at the response to a short circuit.




If $t_2$-$t_1 \leq 0.5x\, t_r$, then two reflections merge as one pulse.

**Figure 8. TDR resolution is defined as $t_2 - t_1 = d$**

For example, the HP 54121T TDR outputs a 35 ps step. A typical "system" risetime is about 40 ps because the scope risetime is limited to 17.5 ps in a 20 GHz scope (and is not infinitely fast). A simple calculation shows a 6 mm resolution in air; and divide by the root of the dielectric constant ($e_r$) for other materials. Some common dielectric constants include 1 for air, 1.4 for microwave cable, 4 for epoxy PC boards, and 9.7 for alumina substrate.

$$\text{Resolution} < \frac{ct_r}{2\sqrt{e_r}}$$

where c = speed of light in a vacuum

In recent years, with the sophistication of microprocessor instrument control, digital signal processing has been incorporated into TDR. The HP 54120-series TDR allows a process called "normalization" which uses time domain information during the calibration to determine the overall TDR system bandwidth rolloff, and construct a variable risetime filter to restore a flat frequency domain response. Normalization has several purposes. First, it removes system errors. Next, one can calculate variable risetime responses to simulate real edge speeds or to increase bandwidth and resolution (to 10 ps). This allows the TDR user to see the reflection which would be present from an ideal step of a user defined edge speed.

As an example, one might be interested in the significance that a coax-to-microstrip connection has on 300 psec GaAs digital signals. The original 40 ps edge indicates reflections. Normalizing the response, one can identify that there is less reflection to a 300 ps step as seen in figure 9.

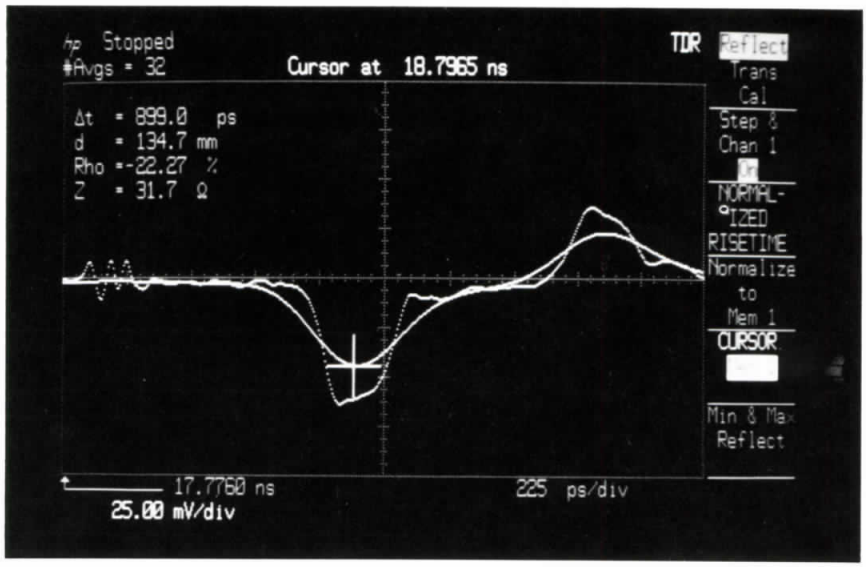



**Figure 9. TDR normalized to 300 ps system speed**

Another important part of analyzing transmission paths is to look at signal integrity along the path, especially at the final destination. Time domain transmission (TDT) measurements are accomplished by introducing the TDR step into a DUT and looking at the resultant signal through the device, described in figure 10. Automatic measurements for propagation delay, gain, and step response are available.

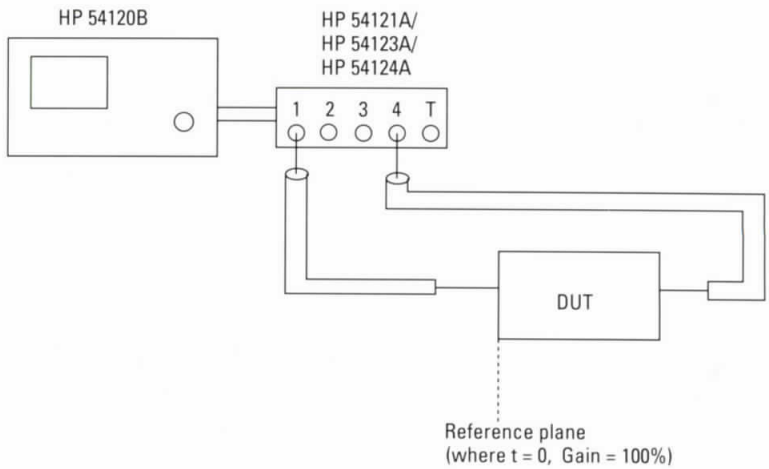



**Figure 10. Time domain transmission**

## Section II - Why is Launching an Issue?

With that brief review behind us, let's move on to the more practical issues of hooking up DUT's for real measurements, and discuss some basic launching issues and their relation to the constraints of a designer concerned with signal integrity.

Let's start by defining the term "launching". This refers to taking the step signal from the channel 1 APC 3.5 coaxial environment (on the scope front panel) and somehow getting that signal into a DUT, whatever it might be.

Why would this be an issue? Take the example of a digital designer who has a transmission path between the output of one chip and the input of another as seen in figure 11. Signals may pass from the chip connector out to microstrip, possibly through an edge connector off the board and into cable, possibly to enter a second board, and then finally to reach the input of the second gate. The designer wants to maintain a certain signal integrity, and may need to look along the path with TDR to analyze and optimize portions of the path. Often it is necessary to inject the TDR step at a point of interest; that point could be one of many environments which may not be simple to connect to.

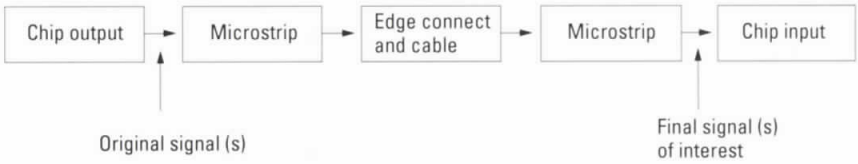



**Figure 11. Typical digital circuit transmission path**

Perhaps the transmission path between the two IC's shown in figure 12 is in question due to some design compromise. Poor transmission paths greatly compound the design task. A way must be found to attach the TDR to find the root of any problem.

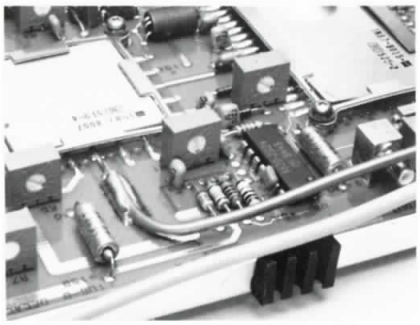


**Figure 12. Testing the chip-to-chip interconnect**

What are the typical signal integrity constraints for the high speed digital designer? Proper 1 and 0 levels with correct timing are the primary factors summarized in table 1. A worst case logic 1 output from a device (Voha) must pass through a transmission path and still maintain an adequate level for the next gate (Viha). This defines a noise margin for the high level, and similar requirements exist for the low level. As edge speeds increase depending on the logic family, transmission line factors like ringing, undershoot, reflections, and crosstalk can all become critical to maintaining these noise margins. Overall, the criteria is fairly forgiving for digital. Notice a 700 mV undershoot on a 1.7 V swing GaAs signal (45% undershoot) is the margin.

**Table 1. Typical logic family voltage specifications (in volts)**

| Logic Type | TTL | Schottky | CMOS | ECL (10K) | ECL (100K) | GaAs |
|---|---|---|---|---|---|---|
| Risetime 10–90, nsec | 4–10 | 1.5–2.5 | 10–100 | 1.5–4 | 0.5–2 | .2–.4 |
| $V_{OHA}$ min | 2.7 | 2.7 | 5.9 | – 0.980 | -1.035 | – 0.2 |
| $V_{IHA}$ min | 2.0 | 2.0 | 4.2 | – 1.105 | -1.165 | – 0.9 |
| $V_{ILA}$ max | 0.8 | 0.8 | 1.2 | – 1.475 | -1.475 | – 1.6 |
| $V_{OLA}$ max | 0.5 | 0.5 | 0.1 | – 1.630 | -1.610 | – 1.9 |
| Noise Margin (High Level) | 0.7 | 0.7 | 1.7 | 0.125 | 0.115 | 0.7 (25C) |

But also notice this 700 mV margin is at 25 degrees Celsius and is very dependent on temperature. The high level noise margin approaches zero as temperature rises as shown in figure 13.

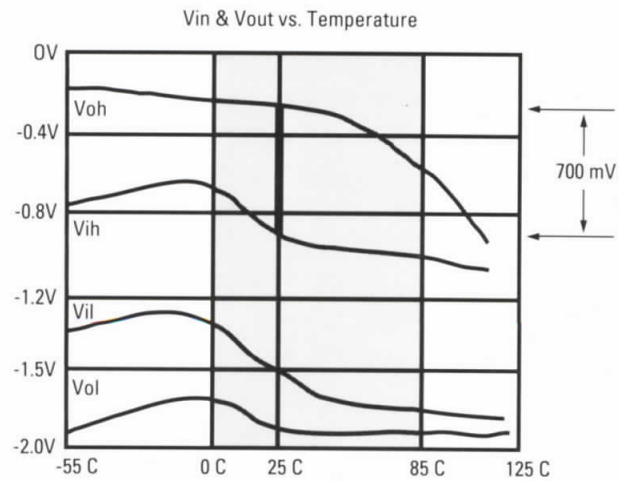



**Figure 13. Typical GaAs performance characteristics**

With such digital design constraints in mind, consider the following typical PC board/backplane measurements and the need for launching. Trace impedance discontinuities are important because they cause reflections and pulse degradation. Unmatched line lengths can cause timing violations, so one measures line propagation delay. Trace bends and termination resistors also cause reflections. A "thru" transmission measurement provides a view of the final pulse fidelity at its destination. Coupling between lines adds noise and is checked with forward and reverse crosstalk measurements. Similar measurements also apply for analog microwave paths, but higher integrity is generally required in such paths, and measurements are often made in the frequency domain. Using a network analyzer, like the HP 8510B, S parameters, frequency response, phase response, and insertion loss can be measured.

Let's now focus attention on each of the major types of transmission path environments, and look at launching options, performance, and typical measurement results for each. Environments will include: PC boards/backplanes, wafers/hybrids, IC packages, connectors, coaxial cables, and balanced lines.

## Section III - PC Boards/ Backplanes

The first area to consider is that of PC boards and backplanes. There are a number of controlled impedance line types, launch options, and resultant TDR performances. Transmission measurements must not be forgotten, including crosstalk measurements. Finally, some typical responses are considered.

There are a number of different controlled impedance line types on PC boards which include: microstrip, coplaner microstrip, stripline, and dual microstrip surrounding lower speed layers (i.e. multi-layer). These are shown in figure 14.

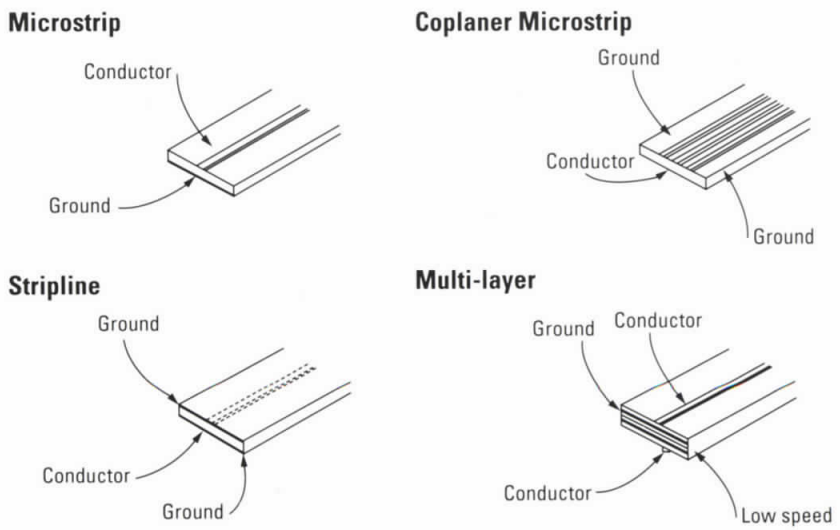



**Figure 14. Controlled impedance lines**

The first is microstrip, where a PC trace of specific width runs above a ground plane, separated by dielectric of fixed thickness to define a controlled impedance. Coplaner microstrip has ground line running on each side of the signal conductor path. In stripline, the conductor is inside the dielectric material and surrounded (top and bottom) by a ground plane. What commonly are found in high speed digital designs are multi-layer PC boards where high speed paths are in microstrip on the outer layers, while low speed digital is on multiple internal layers.

So how is one going to attach to such transmission lines? Major launch options include: semirigid cable or launcher to board edge and semirigid cable or launcher to via holes (Note: in all cases, the signal must be injected at the end of a "T" path.)

When it comes to options, one must generally use semirigid cable or PC board edge connectors (launchers), and connect these either to traces which run out to a board edge or to via holes on the board which attach to the signal path and to ground. The TDR input step must always be launched at the end of a T path.

In the case of using semirigid cable, one must strip back the cable to expose the center conductor and attach a short ground wire (less than 0.5 cm in length). Vias are a convenient method of making access to ground as demonstrated in figure 15.

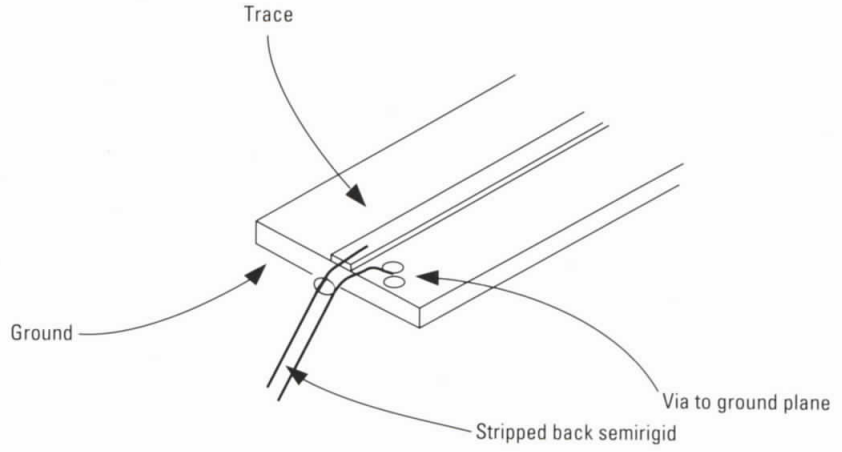



**Figure 15. Semirigid cable launched onto trace and via hole**

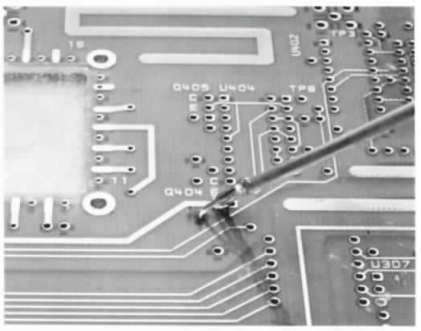


**Figure 16. Semirigid onto trace with via holes**

**Figure 18. Standard SMA/SMB Launchers**

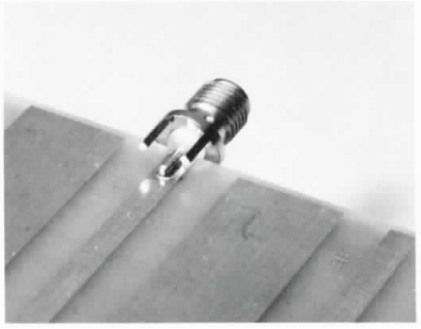


**Figure 19. SMA Edge Launcher**

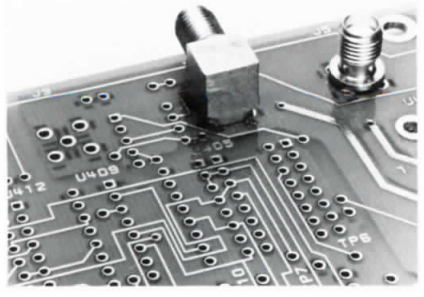


**Figure 20. SMA 90° Launcher**

A semirigid launcher attached to a trace under test with via holes is shown in figure 16. This can be soldered or simply touched to the via holes like a probe. The semirigid provides a good 50 Ω transmission line.

An HP 54121T TDR measurement of the PC trace in figure 16 can be seen in figure 17. One can see the launch point, the length of line, and the PC board's impedance variations.

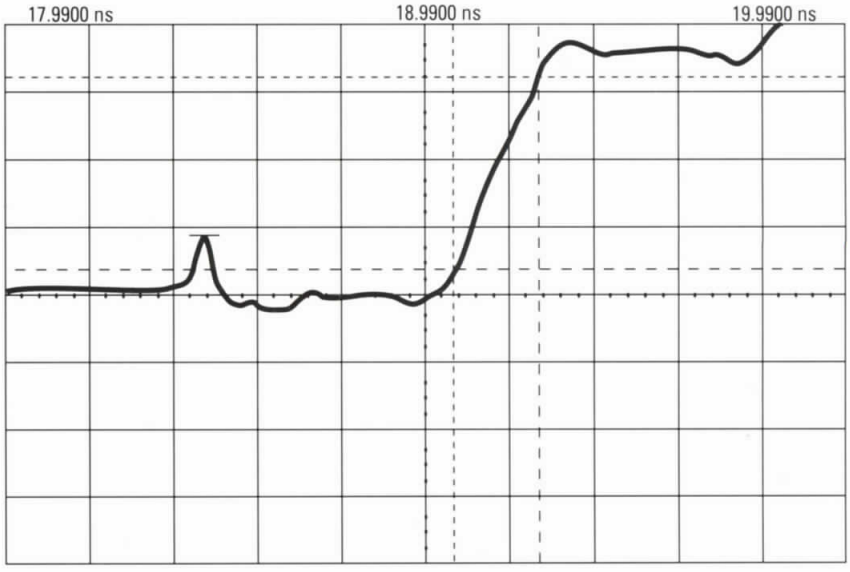



**Figure 17. Launching through a semirigid cable onto trace with via hole**

The other option for attaching TDR to PC traces is through commercially available SMA and SMB board connectors like shown in figure 18. Versions exist for microstrip, coplaner, and microstrip launches.

A view of an edge launch is shown in figure 19.

Another SMA, 90 degree board connector is shown in figure 20.

In terms of required TDR resolution to measure a PC trace, the length of the path of interest must be considered. To see detail, the resolution will define a necessary TDR risetime, and this must be maintained. Various launch techniques will limit this risetime. A number of launchers were compared when attached to short 50 Ω microstrip lines and results summarized in table 2. Signals were introduced to the launcher from the TDR through a 3 foot coaxial cable. The risetime of the open circuit at the end of the microstrip line was observed to approximate the effective TDR risetime when viewing the PC trace. The hybrid and APC 3.5 launchers had such small effects, they were measured directly from the TDR front panel (40 psec) for reference.

**Table 2. Typical PC board launcher performance**

| Type | % Reflect (live through cable) | t rise | Resolution (air cm) | Price ($) |
|---|---|---|---|---|
| 0.025 Square Pin | +16% | 280 psec | 4.2 | <1 |
| SMB 90° | –21% | 200 psec | 3.0 | 8 |
| Semirigid to Trace and Via | +17.5% | 190 psec | 2.9 | 20 |
| SMA 90° | –25% | 170 psec | 2.6 | 9 |
| Semirigid to Edge | +16% | 160 psec | 2.4 | 20 |
| SMA Edge | +5.3% | 110 psec | 1.7 | 7–20 |
| SMA Hybrid 90° | +12% | 80 psec | 1.2 | 10 |
| APC 3.5 Edge | ±0.2% | 40 psec | 0.6 | N/A |

Some practical PC board launch tips include making an effort to design launch points (i.e. vias), launch with 50 Ω (do not use the HP 54006A), and calibrate coaxial near to the launch point.

Turning attention to transmission measurements, one must inject the TDR step in the same way to a DUT but probe signals along the path, primarily at the destination point. Here, the HP 54006A 6 GHz 1 kΩ, 20:1 or 500 Ω, 10:1 resistive divider probe can effectively view fast edge or high frequency signals without disturbing the 50 Ω path signals. Firmware built into the scope channel 4 input interprets propagation delay and gain directly. The HP 54006A probe is shown in figure 21.

**Figure 21. Transmission measurement using the HP 54006A 6 GHz probe**

A special transmission measurement which also uses the TDR step and the channel 4 input is that of crosstalk. Here the step is input to a line adjacent to the line of interest, and coupled energy is viewed on the line of interest. Here variable risetimes with normalization allows the amount of coupling to be determined by the simulation with real edge speeds. Crosstalk mostly happens through capacitance between lines, and coupled energy is a di/dt effect.

Near and far end crosstalk are both of interest, and measurement configurations are shown in figure 22. In all cases the lines must be

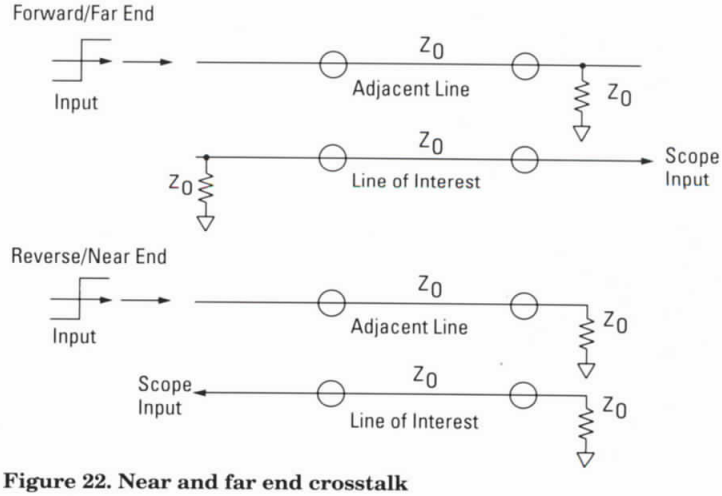



**Figure 22. Near and far end crosstalk**

properly terminated. If lines are 50 Ω, the scope input channels can be used to terminate the DUT line. If not, the line should be properly terminated and the HP 54006A probe can be used to view signals.

Figure 23 contains a typical PC board set of measurements. Notice the launch point, the trace itself, the termination resistor through TDR, and the resultant edge at the terminations resistor through TDT with the 6 GHz probe. But what is typical?

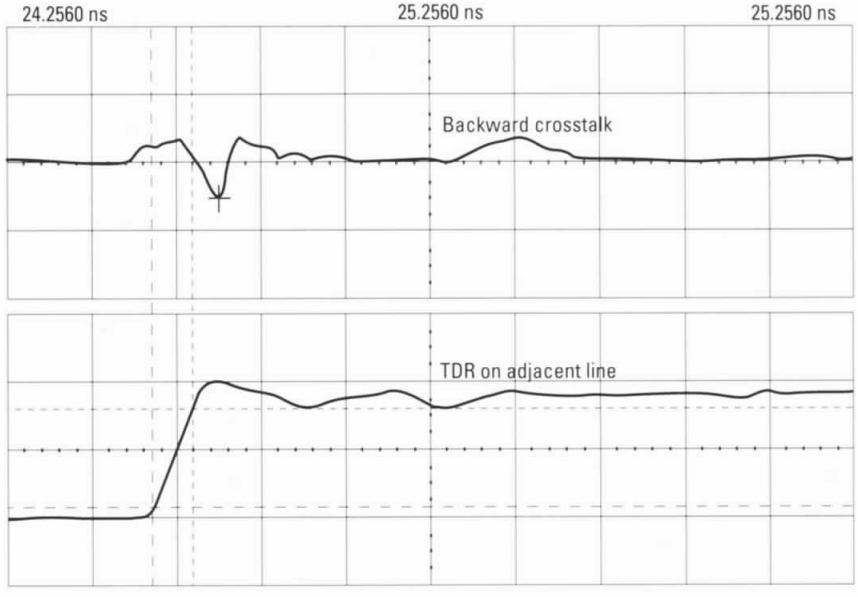



**Figure 23. PC Board microstrip trace crosstalk**

There is not a simple answer to that question for it is very dependent on the application. Some example measurements are presented in table 3 with the live TDR system. Most reflection and crosstalk measurements are between 5% and 25%.

**Table 3. Typical PC trace/backplane responses (50 to 100 Ω environments)**

| DUT | % Reflect* | Crosstalk |
|---|---|---|
| Term Resistor | 10 – 15% | N/A |
| Trace Bend | 5% | N/A |
| Parallel PC Traces | N/A | 1 – 25% |
| Backplane Interface | N/A | 5 – 10% |

*Live, 45 ps tr

## Section IV - Wafer/Hybrid Testing

PC board measurements are fairly simple and do not require very sophisticated techniques for launching due to the large physical dimensions. The next environment area for consideration includes both wafers and hybrids. Each of these environments have similarities to PC boards in some aspects but have much smaller dimensions. Let's look at launching methods and required performance, as well as an actual hybrid measurement.

**Figure 24. Hybrid testing**

Notice that the hybrid in figure 24 is like a miniature PC board with small devices and controlled impedance microstrip lines. Alternate launching techniques are now necessary. Here an SMA to hybrid microstrip line launcher brings signals into the environment.

Options to connect to wafers and hybrids include the 90 degree launcher just shown, coax to microstrip edge adapters, and wafer probing stations with multi-GHz bandwidth, 50 Ω, coplanar probes.

But one first needs to understand the difference between wafers, dies, and hybrids to appreciate the various launching techniques and their application during the stages of creating a wafer, taking a die from the wafer, and placing the die onto a hybrid. A short tutorial follows giving this background, followed by the performance factors.

Initially, a long rod of Silicon is grown, and thin 15-20 mil slices are cut from it. All IC processing is performed on this disk such as diffusing transistors and adding metal layers. This final disk is called a wafer. It may contain several hundred circuits. The hybrid is then sliced up to form "die" which may contain thousands of transistors and components to form an IC.

Now the IC or IC's can be mounted on ceramic thick film along with surface mount resistors, thick film capacitors, or other dies from wafers. This new part is called a "hybrid". Dies are usually connected to the thick film using 1 mil bond wires which are a few millimeters in length.

There are many advantages to testing circuits at wafer level without having to cut the wafer into die or mount die onto ceramic thick film or into packages. These type of wafer measurements require a wafer prober to position probes under a microscope to connection pads. Often normal scope measurements are performed on device outputs at this level.

If cut into die, the die must usually be mounted to ceramic to be tested in the form of a hybrid. The circuit in a hybrid is usually considerably larger than a die circuit since it may contain numerous components interconnected with microstrip.

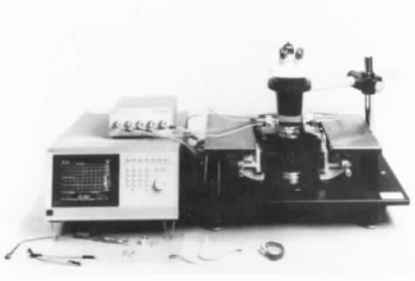


**Figure 25. Wafer probing station**

In both cases of wafers and hybrids, the DUT's are small (< 2-3 cm) so high resolution is required. If the 40 ps TDR risetime can be maintained through the launch this is often adequate resolution. Launchers are best used directly from the TDR front panel and then normalization pushes the risetime quite easily to 20 ps. Probing stations are available which can achieve 20 ps normalized measurements. If one desires to see bond wires to IC's, 10 ps TDR risetimes are necessary, and can be approached with normalization.

A view of a wafer probing station available from Cascade Microtech can be seen in figure 25.

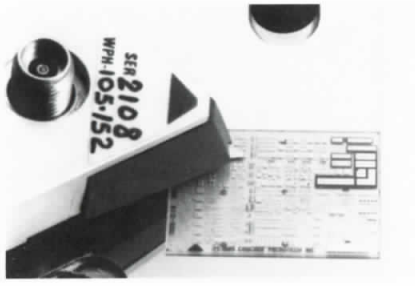



**Figure 26. 50Ω probe tip to hybrid**

Figure 26 shows a 50 Ω probe tip to a hybrid circuit. The DUT here is actually a special hybrid without any active chips called an impedance standards substrate (ISS) and is used for TDR/TDT calibrations. Impedance standards have accuracies as high as 0.1%. This allows calibration all the way to the probe tip.

A coaxial to microstrip edge adapter in a microwave test fixture is shown in figure 27. This offers extremely high quality launching capabilities. The microwave test fixture allows positioning of the adapter to the hybrid edge microstrip trace.

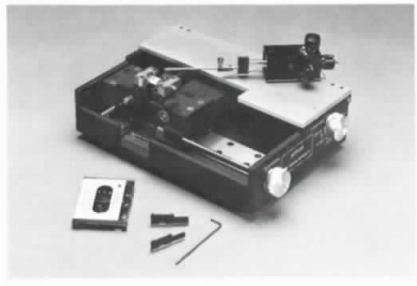


**Figure 27. Coaxial to microstrip adaptor**

Earlier we looked at a hybrid with a 90 degree SMA launcher into a microstrip trace. Here is the result, with a HP 54121T showing a length of non-50Ω path from pad to pad. In fact the impedance from 55.4Ω to 108Ω when formalized to a 20ps risetime shown in figure 28. Normalization has been used first to increase resolution by decreasing the risetime to 20 ps. Next, normalization calculated the reflections that would be seen from a perfect 100 ps step. This path was designed to have less than 5% reflections to 100 ps. The cursor reads 4.1% which is well within specification.

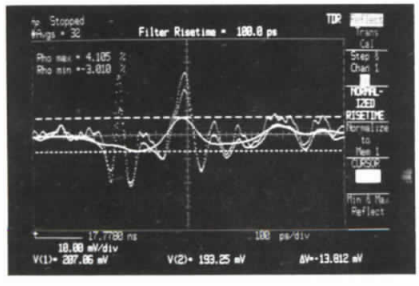



**Figure 28. Hybrid measurement**

## Section V - IC Package Testing

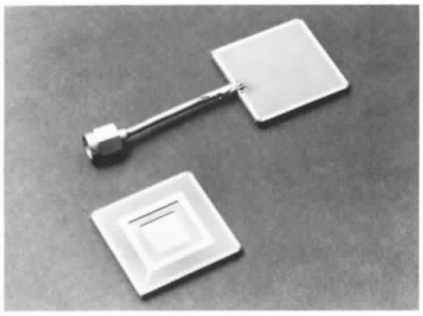


**Figure 29. Short semirigid on IC package pad**

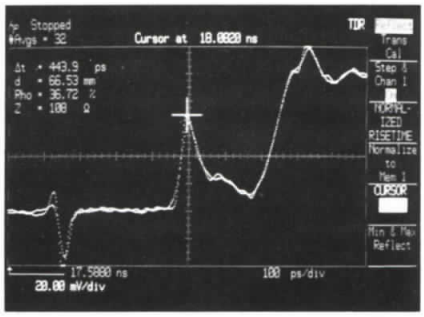



**Figure 30. TDR Response to IC package path**

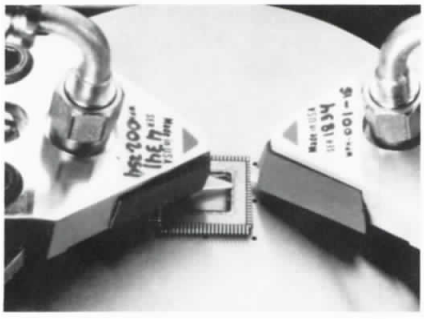


**Figure 31. GHz probes to IC package**

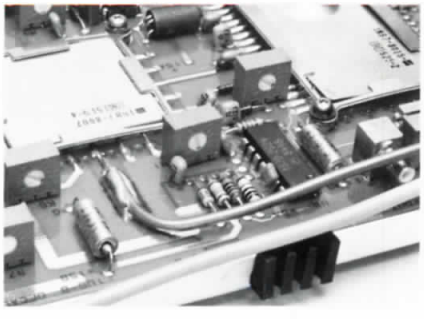


**Figure 32. IC package test**

Another important area for TDR and TDT measurements is the analysis of IC packages. High speed digital IC's in die form can be placed on ceramic or placed into a package. The package transmission path in the case of GaAs IC's must maintain edge speeds in the 100's of picoseconds. What launch options, performance and typical responses might one expect?

Launch options include: short semirigid (1-3 cm), short leads (2-4 mm) to pin or pad, GHz coplaner probes to pin or pad, and mounting of IC's into the real environment and launching into microstrip. In cases where a designer needs to know the package performance in a specific application, the package must be mounted into its real environment and the launch is performed in microstrip at a distance far enough from the package to see the package path reflections.

TDR and launch performance in this application area are also completely dependent on the package size, and for paths > 1 cm, a 40 ps TDR measurement is adequate. For smaller path packages, normalizing to 20 ps covers most needs. Semirigid gives limited performance but is very inexpensive. The wafer prober station gives high performance but is considerably more expensive. Mounting a package into its real environment will be somewhat limited in bandwidth due to launching into PC board microstrip, but will best show true performance.

A measurement on a surface mount leadless IC package was taken with a short semirigid cable as shown in figure 29 and normalized down to 16 ps risetime at the SMA input to the semirigid launcher. This is an example where normalization allows very high resolution.

Results with the HP 54121T, showing the length and 108 Ω maximum impedance of the non-50 Ω path from pad to pad, can be seen in figure 30.

High bandwidth GHz probes, shown in figure 31, are being used for IC package transmission line analysis. Probes could be part of a wafer probing station or mounted through other means.

Finally, a view of a mounted IC package with semirigid cable launched directly into an input pad is shown in figure 32.

## Section VI - Connector Interfaces

Many TDR tests are performed on connectors, either as a specific DUT or as part of a complete transmission path. Simple adapters attached to the HP 54121A front panel provide an excellent launch method. Next best is a short cable to serve as an adapter.

A wide range of performance DUT's dictate wide TDR needs, but most high end connector types like APC 3.5, K, or HP 2.4 need front panel calibrations and 20 ps or faster normalizations to see individual connector structures. A 20 ps normalization achieves 3 mm resolution in air. With a careful calibration in the averaged mode, 10 ps normalizations are possible from the front panel.

Table 4 contains a summary of low to high end connectors and TDR responses.

**Table 4. Connector performance summary**

| Type | BW (GHz) | Percent (Live) | Reflection 200 psec | Reflection 1 nsec |
|---|---|---|---|---|
| .025 square pin | | 12.7 | 5.8 | 0.3 |
| BNC | 2 | 14.6 | 5.4 | 0 |
| SMB | 10 | 8.0 | 3.3 | 0 |
| N | 18 | N/A | N/A | N/A |
| APC 7 | 18.5 | 1.0 | 0 | 0 |
| SMA | 26 | 3.8 | 0.5 | 0 |
| APC 3.5 | 34 | 1.2 | 0 | 0 |
| K | 44 | N/A | N/A | N/A |
| HP 2.4 | 50 | N/A | N/A | N/A |

## Section VII - Cable Testing

Another DUT area includes various cable types. These include unbalanced coaxial lines and balanced twisted pair lines, each with different launch options. Differential TDR techniques are required for twisted pairs and will be described.

Cable testing presents some interesting considerations. If the DUT is a coaxial unbalanced line with a connector, launching is usually accomplished with a simple adapter. Live 40 ps TDR responses are almost always adequate in resolution due to the typically long DUT length. For example, a 40 ps TDR risetime achieves 3 mm resolution in a coaxial cable where Er = 1.7.

However, resolution degrades as one looks further and further down the line. One must also ensure that the TDR rep rate is slow enough to allow the TDR step to propagate to the end of the cable and back to the scope before the step is turned off. For a 1000 foot (300 m) cable, the rep rate should be adjusted from 500 kHz down to 250 kHz.

## Section VIII - Balanced Lines

Balanced DUT cables such as twisted pair and twin lead (both shielded and unshielded) present a different measurement problem. Here, one must either present a differential step source to the DUT and observe Channel 1 - Channel 2 on the scope, or use a single pulse generator and again observe channel 1 - channel 2. This method takes advantage of the differential mode present in a single ended pulse source. One can check for imbalance with the single pulse generator method by reversing the leads to the DUT and identifying any changes in the trace.

The diagram in figure 33 represents the equivalent circuit of the single pulse generator present in channel 1 of the HP 54121T, and the normal scope channel 2. Each is attached to 50 Ω cables, and the center conductor of each cable is attached to the balanced DUT. It can be shown that with this configuration, one can perform differential TDR measurements.

First consider that differential TDR means stimulating a DUT with an effective differential pulse, and measuring the differential impedance by observing reflections. One can create this differential pulse by carefully synchronizing two pulse generators of opposite polarity and identical pulse shape, and observing channel 1 - channel 2.

Now, let's consider the single step generator in the channel 1 line of the HP 54121A with amplitude represented by "A", and work toward a differential TDR solution.

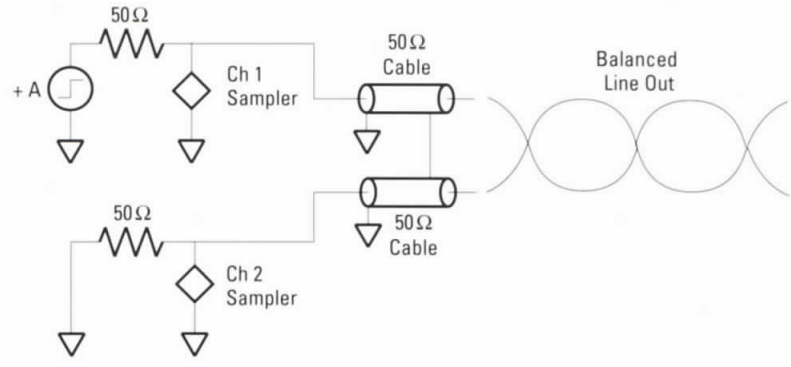



**Figure 33. Differential TDR**

If we redraw the single step source as three sources shown in figure 34, the first one common mode with amplitude "+ 1/2 A" driving a differential pair of sources of amplitudes "+ 1/2 A" and "- 1/2 A", we have an equivalent circuit which contains the differential pair that is desired for differential TDR. By looking at channel 1 - channel 2, the common mode element is subtracted leaving only the differential response, as long as the DUT is truly balanced. If an imbalance exists on the line, it will be identified by switching the leads to the DUT and noting the regions in the trace which differ. The single source is very useful for differential TDR if used in conjunction with channel 2.

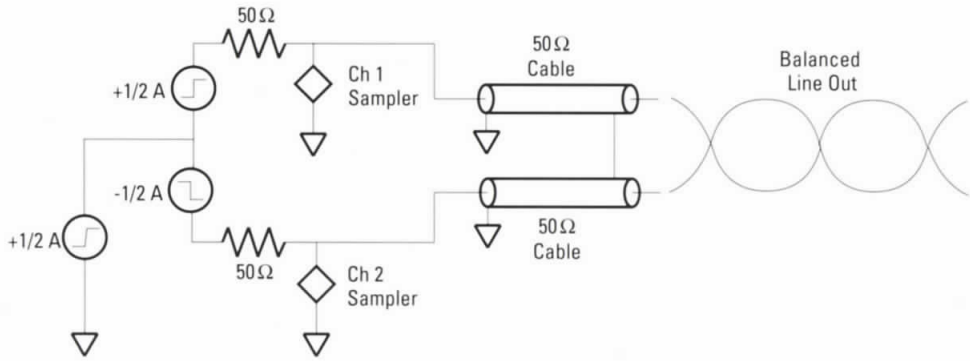



**Figure 34. Differential TDR**

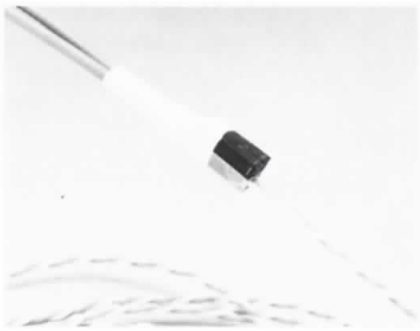


**Figure 35. Connecting to a twisted pair**

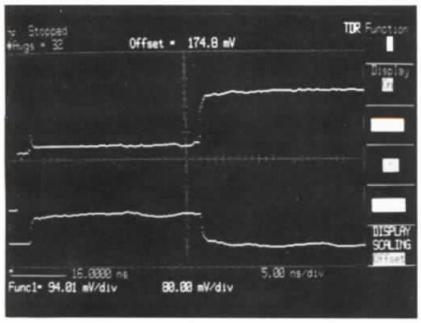



**Figure 36. Twisted pair measurement**

Launching can be accomplished by using dual 50 Ω coaxial cables attached to a standard 0.025 in. square pin connector, or by soldering to dual semirigid line center conductors. Live TDR traces provide more than adequate resolution to see twist density variations and resultant differential impedance changes. If a balanced line DUT is grounded, the DUT ground is attached to ground on the semirigid cables.

A view of the 0.025 square pin technique is seen in figure 35. This adapter is available from W.L. Gore and Associates and provided a 120 ps TDR system risetime (14 mm resolution, Er = 1.7).

The front panel TDR trace in figure 36 has identified the differential impedance and prop delay through a high speed computer backplane twisted pair cable.

One quickly realizes that there are many types of DUT's with varied performance and launching techniques.

## Section IX - Calibration Techniques

Here are some basic tips on proper calibrations. Once the scope is warmed up (30 minutes), perform a vertical calibration. This linearizes the entire scope vertical system and optimizes dc accuracy, important for impedance calculations.

Next, calibrate coaxial (or coplanar on a wafer probing station standards substrate), because "short" and "50 Ω" calibrations are very difficult on the end of semirigid or on a PC trace. If normalizing faster than 20 ps, one should use precision APC 3.5 shorts and loads.

If it is important that the TDR cursor read the distance from an exact point, then it is necessary to perform a "short" cal at that point, even if it is at a semirigid tip or a PC trace. Copper tape can be used for the short. The 50 Ω cal should still be performed at the nearest coaxial point with a coaxial load. Caution should be taken if normalizing, since the normalized response will correct for the frequency roll-off measured in the short-circuit, and this may be an artificial effect not present in the actual measurement connection to a device.

## Section X - Non 50 Ω Environments

Finally, there is a misconception that non-50 Ω measurements are inaccurate with a 50 Ω TDR system. There is a major reflection at the 50 Ω to non-50 Ω launch, but the size of this reflection is in fact what defines the impedance measurement on screen, and it is based on the full size TDR step being present in 50 Ω environment up to that point. Therefore, always launch from 50 Ω unless it is crucial that no major reflection be near the DUT. This can be the case if small changes in the DUT impedance are under scrutiny.

After the 50 Ω to non-50 Ω reflection, second reflection errors will be present when looking at deviations in the DUT impedance from its nominal value. Such errors must be treated with a correction table as shown in figure 37.

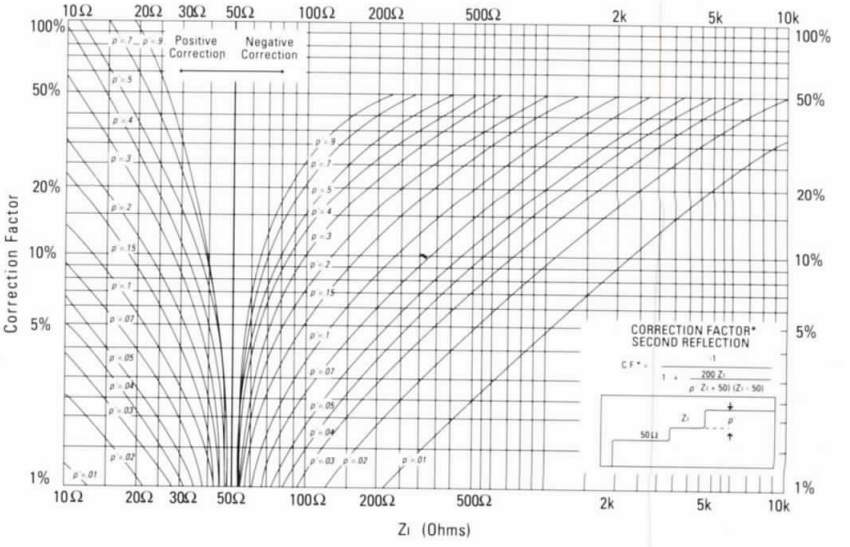



**Figure 37. Second reflection correction factor**

If using normalization, one must maintain a 50 Ω path on screen up to the Cal point since this average voltage is used as a 50 Ω reference.

Finally, since software for the live cursor is always defined to a 50 Ω calibration, it is best to use a 50 Ω load for the calibration.

## Conclusion

What have we learned? First, the TDR is an excellent tool to transmission paths to ensure adequate signal integrity, especially with calibration and normalization capabilities now offered.

It was also seen that the microwave or high speed digital designer has design constraints that often lead to the analysis of a particular part of a DUT. That means many possible environment types might be evaluated and a knowledge of different launching techniques and their performance is crucial to use TDR effectively.

The transmission measurement must not be forgotten, since it really shows the final effects of a complete transmission path on signals and effects from crosstalk.

Normalization is a powerful feature with the capability to test with higher resolution or to see reflection or transmission characteristics at "real" edge speeds. Familiarity with practical "helpful hints" can then further enhance measurement accuracy.

HEWLETT PACKARD

**United States:**
Hewlett-Packard Company
4 Choke Cherry Road
Rockville, MD 20850
(301) 670-4300

Hewlett-Packard Company
5201 Tollview Drive
Rolling Meadows, IL 60008
(708) 255-9800

Hewlett-Packard Company
5161 Lankershim Blvd.
No. Hollywood, CA 91601
(818) 505-5600

Hewlett-Packard Company
2015 South Park Place
Atlanta, GA 30339
(404) 955-1500

**Canada:**
Hewlett-Packard Ltd.
6877 Goreway Drive
Mississauga, Ontario L4V 1M8
(416) 678-9430

**European Headquarters:**
Hewlett-Packard S.A.
150, Route du Nant d'Avril
1217 Meyrin 2
Geneva-Switzerland
41/22 780-8111

**Japan:**
Yokogawa Hewlett-Packard Ltd.
15-7, Nishi Shinjuku 4 Chome
Shinjuku-ku,
Tokyo 160, Japan
(03) 5371-1351

**Latin America:**
Latin American Region Headquarters
Monte Pelvoux No.111
Lomas de Chapultepec
11000 Mexico, D.F. Mexico
(525) 202-0155

**Australia/New Zealand:**
Hewlett-Packard Australia Ltd.
31-41 Joseph Street
Blackburn, Victoria 3130
Melbourne, Australia
(03) 895-2895

**Far East:**
Hewlett-Packard Asia Ltd.
22/F Bond Centre, West Tower
89 Queensway, Central, Hong Kong
848-7777

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